Connection Diagrams (Continued)

Pin Assignments for DIP and SOIC

CD4060BC

V_{DD} 16, Q_{10} 15, Q_8 14, Q_9 13, RESET 12, $\phi 1$ 11, $\overline{\phi 0}$ 10, $\phi 0$ 9

Q_{12} 1, Q_{13} 2, Q_{14} 3, Q_6 4, Q_5 5, Q_7 6, Q_4 7, V_{SS} 8

Top View

Schematic Diagrams

CD4020BC

$\phi 1$ 10

11 RESET

8 = V_{SS}

16 = V_{DD}

CD4040BC

$\phi 1$ 10

11 RESET

8 = V_{SS}

16 = V_{DD}




Absolute Maximum Ratings (Note 1)

(Note 2)

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to V_{DD} +0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Package Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions

Supply Voltage (V_{DD})	+3V to +15V
Input Voltage (V_{IN})	0V to V_{DD}
Operating Temperature Range (T_A)	−40°C to +85°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20			20		150	µA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40			40		300	µA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80			80		600	µA
V_{OL}	LOW Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	HIGH Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	LOW Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	HIGH Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	LOW Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	HIGH Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	µA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	µA

Note 3: Data does not apply to oscillator points ϕ_0 and $\overline{\phi_0}$ of CD4060BC. I_{OH} and I_{OL} are tested one output at a time.





TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS030D – Revised December 2003

CD4020B, CD4024B, CD4040B Types

CMOS Ripple-Carry Binary Counter/Dividers

High-Voltage Types (20-Volt Rating)

CD4020B – 14 Stage
CD4024B – 7 Stage
CD4040B – 12 Stage

■ CD4020B, CD4024B, and CD4040B are ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of a counter advances one count on the negative transition of each input pulse; a high level on the RESET line resets the counter to its all zeros state. Schmitt trigger action on the input-pulse line permits unlimited rise and fall times. All inputs and outputs are buffered.

The CD4020B and CD4040B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes). The CD4040B type also is supplied in 16-lead small-outline packages (M and M96 suffixes).

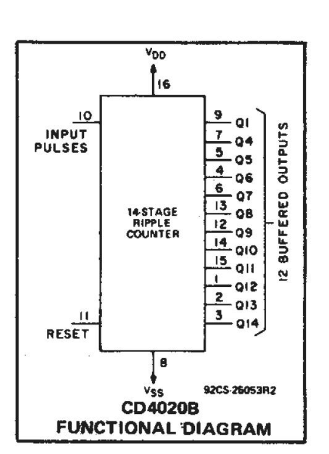
The CD4024B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

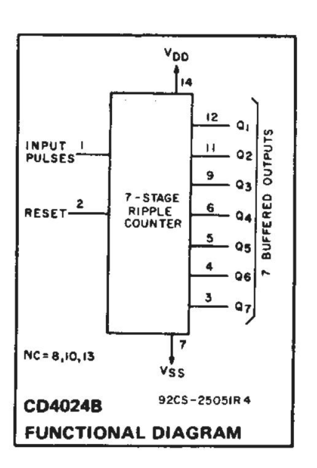
- Medium-speed operation
- Fully static operation
- Buffered inputs and outputs
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- Fully static operation
- Common reset
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range): 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits



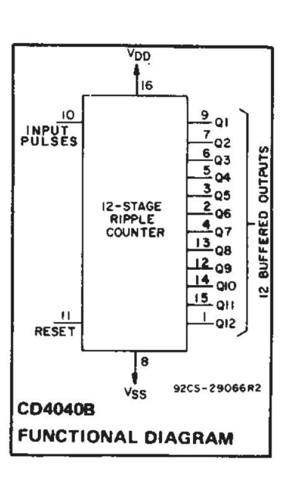
CD4020B FUNCTIONAL DIAGRAM



CD4024B FUNCTIONAL DIAGRAM

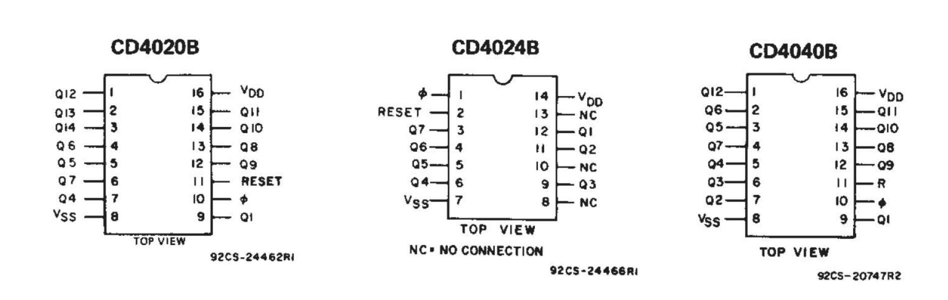
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) .... –0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS .... –0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT .... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = –55°C to +100°C 500mW
For T_A = +100°C to +125°C .... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) .... –55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... –65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max .... +265°C



CD4040B FUNCTIONAL DIAGRAM

TERMINAL ASSIGNMENTS





RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		V_{DD}	Min.	Max.	UNITS
Supply Voltage Range (at T_A = Full Package-Temperature Range)			3	18	V
Input-Pulse Frequency,	f_ϕ	5 10 15	– – –	3.5 8 12	MHz
Input-Pulse Width,	t_W	5 10 15	140 60 40	– – –	ns
Input-Pulse Rise or Fall Time,	$t_{r\phi}$, $t_{f\phi}$	5 10 15	Unlimited		μs
Reset Pulse Width,	t_W	5 10 15	200 80 60	–	ns
Reset Removal Time,	t_{REM}	5 10 15	350 150 100	– – –	ns

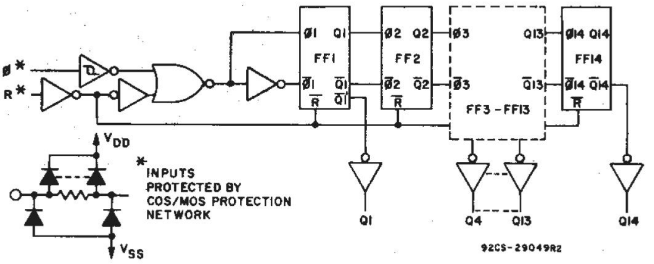


Fig. 1 – Logic diagram for CD4020B.

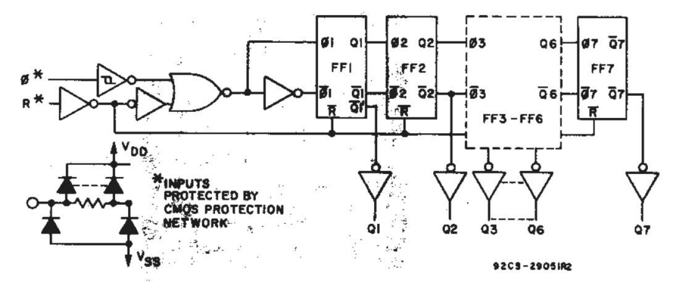


Fig. 2 – Logic diagram for CD4024B.

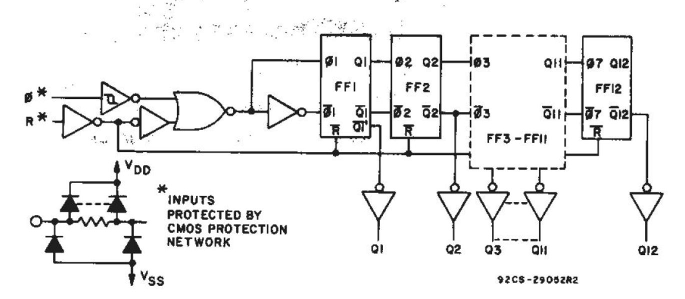


Fig. 3 – Logic diagram for CD4040B.

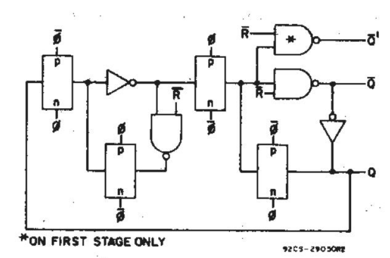


Fig. 4 – Detail of typical flip-flop stage.

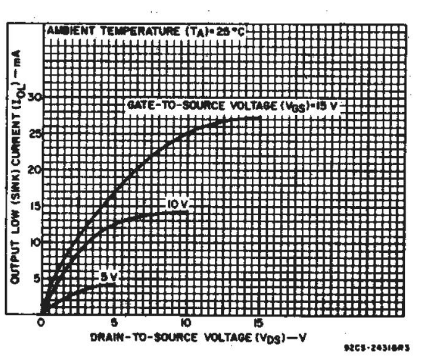


Fig. 5 – Typical output low (sink) current characteristics.

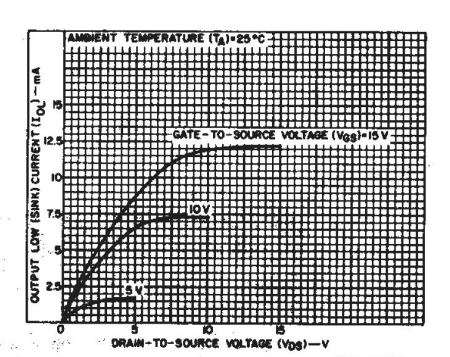


Fig. 6 – Minimum output low (sink) current characteristics.

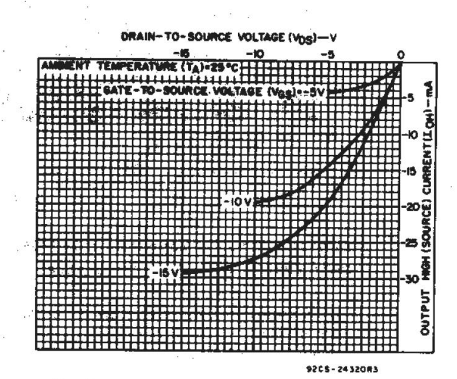
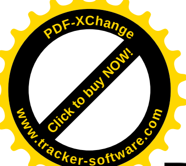
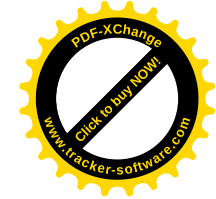
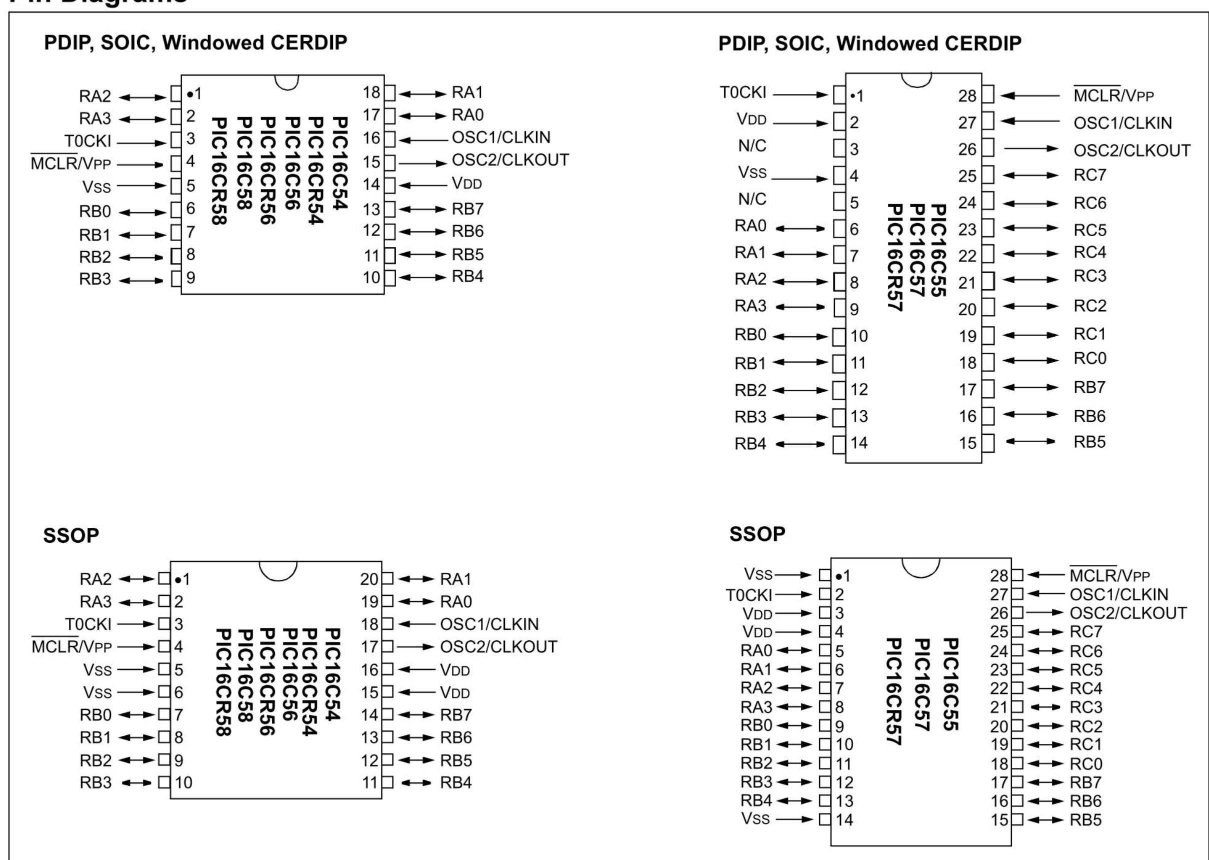


Fig. 7 – Typical output high (source) current characteristics.





Pin Diagrams



Device Differences

Device	Voltage Range	Oscillator Selection (Program)	Oscillator	Process Technology (Microns)	ROM Equivalent	MCLR Filter
PIC16C54	2.5-6.25	Factory	See **Note 1**	1.2	PIC16CR54A	No
PIC16C54A	2.0-6.25	User	See **Note 1**	0.9	—	No
PIC16C54C	2.5-5.5	User	See **Note 1**	0.7	PIC16CR54C	Yes
PIC16C55	2.5-6.25	Factory	See **Note 1**	1.7	—	No
PIC16C55A	2.5-5.5	User	See **Note 1**	0.7	—	Yes
PIC16C56	2.5-6.25	Factory	See **Note 1**	1.7	—	No
PIC16C56A	2.5-5.5	User	See **Note 1**	0.7	PIC16CR56A	Yes
PIC16C57	2.5-6.25	Factory	See **Note 1**	1.2	—	No
PIC16C57C	2.5-5.5	User	See **Note 1**	0.7	PIC16CR57C	Yes
PIC16C58B	2.5-5.5	User	See **Note 1**	0.7	PIC16CR58B	Yes
PIC16CR54A	2.5-6.25	Factory	See **Note 1**	1.2	N/A	Yes
PIC16CR54C	2.5-5.5	Factory	See **Note 1**	0.7	N/A	Yes
PIC16CR56A	2.5-5.5	Factory	See **Note 1**	0.7	N/A	Yes
PIC16CR57C	2.5-5.5	Factory	See **Note 1**	0.7	N/A	Yes
PIC16CR58B	2.5-5.5	Factory	See **Note 1**	0.7	N/A	Yes

Note 1: If you change from this device to another device, please verify oscillator characteristics in your application.

Note: The table shown above shows the generic names of the PIC16C5X devices. For device varieties, please refer to Section 2.0.

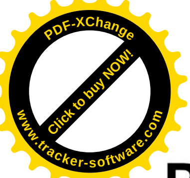




TABLE 16-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC16C58A-04	PIC16C58A-10	PIC16C58A-20	PIC16LC58A-04
RC	VDD: 3.0V to 6.25V IDD: 2.5 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 1.8 mA typ. at 5.5V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 1.8 mA typ. at 5.5V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 0.5 mA typ. at 5.5V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.
XT	VDD: 3.0V to 6.25V IDD 2.5 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 1.8 mA typ. at 5.5V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 1.8 mA typ. at 5.5V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 3.0V to 6.25V IDD: 0.5 mA typ. at 5.5V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 4.0 MHz max.
HS	N/A	VDD: 4.5V to 5.5V IDD: 8.0 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 10 MHz max.	VDD: 4.5V to 5.5V IDD: 17 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 20 MHz max.	N/A
LP	VDD: 3.0V to 6.25V IDD: 15 μA typ. at 32kHz, 3.0V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 200 kHz max.	N/A	N/A	VDD: 2.5V to 6.25V IDD: 28 μA max. at 32kHz, 2.5V WDT dis IPD: 4.0 μA max. at 2.5V WDT dis Freq: 200 kHz max.

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

OSC	PIC16C58A/JW	PIC16LV58A-02
RC	VDD: 3.0V to 6.25V IDD: 2.5 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 2.0V to 3.8V IDD: 0.5 mA typ. at 3.0V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 2.0 MHz max.
XT	VDD: 3.0V to 6.25V IDD 2.5 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 4.0 MHz max.	VDD: 2.0V to 3.8V IDD: 0.5 mA typ. at 3.0V IPD: 0.25 μA typ. at 3.0V WDT dis Freq: 2.0 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 17 mA max. at 5.5V IPD: 4.0 μA max. at 3.0V WDT dis Freq: 20 MHz max.	N/A
LP	VDD: 2.5V to 6.25V IDD: 28 μA max. at 32kHz, 2.5V WDT dis IPD: 4.0 μA max. at 2.5V WDT dis Freq: 200 kHz max.	VDD: 2.0V to 3.8V IDD: 27 μA max. at 32kHz, 2.5V WDT dis IPD: 4.0 μA max. at 2.5V WDT dis Freq: 200 kHz max.

The shaded sections indicate oscillator selections which should work by design, but are not tested. It is recommended that the user select the device type from information in unshaded sections.

 Preliminary





16.1 DC Characteristics: PIC16C58A-04, 10, 20 (Commercial) PIC16C58A-04I, 10I, 20I (Industrial)

DC Characteristics Power Supply Pins	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD					
XT, RC and LP options		3.0	—	6.25	V	
HS option		4.5	—	5.5	V	
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD rise rate to ensure Power-On Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)	IDD					
XT and RC(4) options		—	1.9	2.5	mA	FOSC = 4.0 MHz, VDD = 5.5V
HS option		—	2.5	8.0	mA	FOSC = 10 MHz, VDD = 5.5V
		—	4.7	17	mA	FOSC = 20 MHz, VDD = 5.5V
LP option, Commercial		—	15	31	µA	FOSC = 32 kHz, VDD = 3.0V, WDT disabled
LP option, Industrial		—	18	39	µA	FOSC = 32 kHz, VDD = 3.0V, WDT disabled
Power Down Current(5)	IPD					
Commercial		—	4.0	12	µA	VDD = 3.0V, WDT enabled
		—	0.25	4.0	µA	VDD = 3.0V, WDT disabled
Industrial		—	5.0	14	µA	VDD = 3.0V, WDT enabled
		—	0.3	5.0	µA	VDD = 3.0V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to Vss, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.

5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

